Guidelines

- Closed book and notes.
- One-page information sheet allowed.
- There are some useful formulas in the end of the exam.
- The values of common parameters are listed at the beginning of next page.
Please use the following parameters for all problems unless specified otherwise:
\( \phi_{n^+} = 550 \text{ mV}, \ \phi_{p^+} = -550 \text{ mV}, \ V_{th} = 26 \text{ mV} \)
\( \varepsilon_{Si} = 11.7, \ \varepsilon_{SiO_2} = 3.9, \ \varepsilon_0 = 8.854 \times 10^{-14} \text{ F/cm}, \)
\( q = 1.6 \times 10^{-19} \text{ C}, \ n_i = 10^{10} \text{ cm}^{-3}. \)

(1) Consider a silicon PN junction diode with an N-doping concentration of \( 10^{16} \text{ cm}^{-3} \) and a P-doping concentration of \( 10^{18} \text{ cm}^{-3} \). Their cross-sectional area of the diode is 100 \( \mu\text{m}^2 \). Assume the reverse saturation current of the diode is \( 10^{-14} \text{ Amp} \). The diode is forward biased at 0.7V.
   a) [10 pt] Find the dynamic resistance at this bias.
   b) [10 pt] Find the depletion capacitance at this bias.

(2) Consider a MOS capacitor with a P+ polysilicon gate and an N-doped substrate with a doping concentration of \( 10^{16} \text{ cm}^{-3} \). The thickness of the oxide is 20 nm.
   a) [10 pt] Find the threshold voltage.
   b) [10 pt] Which mode is the MOS capacitor in when its gate is biased at 1 V?
   c) [10 pt] What is the maximum capacitance per unit area?
   d) [10 pt] What is the minimum capacitance per unit area?

(3) [10 pt] For the MOS capacitor in Problem (2), plot the charge density distribution as a function of position when the gate is biased at -2V. Please be as quantitative as possible. Show the positions of all charges, and show the magnitude and polarity of the charges.

(4) [10 pt] If the P+ gate of the MOS capacitor in Problem (2) is replaced by a metal whose electrostatic potential is 0V. What is the threshold voltage of the new MOS capacitor?

(5) Consider an N-MOSFET with an N+ polysilicon gate on P-type substrate (\( N_a = 10^{17} \text{ cm}^{-3} \)). The source is grounded, and the drain is biased at 5V. The transistor has a gate length of 1 \( \mu\text{m} \), and a width of 10 \( \mu\text{m} \). The thickness of gate oxide is 10 nm. For simplicity, assume the channel-length modulation parameter \( \lambda = 0 \).

   a) [10 pt] At what gate voltage does the transistor turn on, i.e., start to have significant current flowing between source and drain?
   b) [10 pt] Find the drain current when the gate is biased at 2V.
Some equations

Mass-action law \[ n \times p = n_i^2(T) \]

Resistivity: \[ \rho_n = \frac{1}{\sigma_n} = \frac{1}{q \mu_n N_{d,eff}} \]

Resistance: \[ R = \frac{\rho L}{Wt} = \left( \frac{\rho}{t} \right) \left( \frac{L}{W} \right) = R_{sq} \left( \frac{L}{W} \right) \]

Total current (e\(^-\)): \[ J = J_{\text{drift}} + J_{\text{diff}} = q \mu_n n E + q D_n \frac{dn}{dx} \]

Gauss’s law: \[ \oint \mathbf{E} \cdot d\mathbf{S} = \frac{Q}{\varepsilon} \quad Q = CV \quad E = -\frac{d\phi}{dx} \]

Depletion layer: \[ X_{d0} = x_{p0} + x_{n0} = \sqrt{\frac{2 \varepsilon_s \phi_{bi}}{q} \left( \frac{1}{N_a} + \frac{1}{N_d} \right)} \quad X_d(V_D) = X_{d0} \sqrt{1 - \frac{V_D}{\phi_{bi}}} \]

pn depletion layer capacitance: \[ C_j = \frac{q N_a x_{p0}}{2 \phi_{bi} \sqrt{1 - \frac{V_D}{\phi_{bi}}}} = \frac{C_{j0}}{\sqrt{1 - \frac{V_D}{\phi_{bi}}}} \]

pn diffusion current \[ J_{\text{diff}} = q n_i^2 \left( \frac{D_p}{N_d W_n} + \frac{D_n}{N_w W_p} \right) \left( \frac{q V_D}{e kT} - 1 \right) \]

Diffusion capacitance: \[ C_d = \frac{1}{2} \frac{q l_D}{kT} \tau \]
Threshold voltage (NMOS)

\[ V_{Tn} = V_{FB} - 2\phi_p + \frac{1}{C_{ox}} \sqrt{2q\varepsilon_s N_a (-2\phi_p)} \]

\[ \phi_p = -\frac{kT}{q} \ln \frac{N_a}{n_i} \]

\[ V_{Tn} = V_{TN0} + \gamma \sqrt{V_{SB} - 2\phi_p} - \sqrt{-2\phi_p} \]

NMOS equations:

\[ I_D = 0, \quad V_{GS} < V_{Tn} \]

\[ i_D = \frac{W}{L} \mu C_{ox} \left( V_{GS} - V_{Tn} - \frac{V_{DS}}{2} \right) V_{DS} (1 + \lambda V_{DS}), \quad V_{GS} > V_{Tn}, \quad V_{DS} < V_{GS} - V_{Tn} \]

\[ i_D = \frac{W}{L} \mu C_{ox} \left( V_{GS} - V_{Tn} \right)^2 (1 + \lambda V_{DS}), \quad V_{GS} > V_{Tn}, \quad V_{DS} > V_{GS} - V_{Tn} \]

MOS capacitances in saturation \( C_{gs} = (2/3)WL C_{ox} + C_{ov} \)

\( C_{ov} = L_D W C_{ox} \)

MOS signal parameters:

\[ g_m = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_{V_{GS}, V_{DS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{Tn}) (1 + \lambda V_{DS}) \approx \mu C_{ox} \frac{W}{L} (V_{GS} - V_{Tn}) \]

\[ r_0 = \left( \frac{\partial i_D}{\partial V_{DS}} \right|_{V_{GS}, V_{DS}} \right)^{-1} \approx \frac{1}{\lambda I_{DS}} \]

\[ g_{mb} = \left. \frac{\partial i_D}{\partial V_{BS}} \right|_{Q} = \frac{\gamma g_m}{2 \sqrt{-V_{BS} - 2\phi_p}} \]
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q := 1.6 \cdot 10^{-19} 
n_i := 10^{10} 
V_{th} := 0.026 

\varepsilon_0 := 8.854 \cdot 10^{-14} 
\varepsilon_s := 11.7 \cdot \varepsilon_0 
\varepsilon_{ox} := 3.9 \cdot \varepsilon_0 

\mu_m := 10^{-4} 
\mu_n := 10^{-7} 
mV := 10^{-3} 

\mu_n := 1450 \text{ cm}^2/\text{V-sec}

(1) (a) 

\text{Is} := 10^{-14} 

\begin{align*}
\text{Id}(V_d) & := \text{Is} \left( \exp \left( \frac{V_d}{V_{th}} \right) - 1 \right) \\
\text{Id}(0.7) & = 4.927 \times 10^{-3} \\
\text{r}_d & := \frac{V_{th}}{\text{Id}(0.7)} \quad \text{r}_d = 5.278 \ \Omega
\end{align*}

(b) 

\text{Nd} := 10^{16} \quad \text{Na} := 10^{18} \quad \text{Area} := 100 \cdot \mu \text{m}^2 

\phi_n := 60 \cdot \text{mV} \cdot \log \left( \frac{\text{Nd}}{\text{n}_i} \right) 
\phi_n = 0.36 

\phi_p := -60 \cdot \text{mV} \cdot \log \left( \frac{\text{Na}}{\text{n}_i} \right) 
\phi_p = -0.48 

\phi_b := \phi_n - \phi_p 
\phi_b = 0.84 

\text{xd}(V_d) := \sqrt{\frac{2 \cdot \varepsilon_s \cdot (\phi_b - V_d)}{q} \cdot \frac{1}{\text{Na}} + \frac{1}{\text{Nd}}} 
\text{xd}(0.7) = 1.353 \times 10^{-5} 

\text{Cj} := \frac{\varepsilon_s}{\text{xd}(0.7)} \cdot \text{Area} 
\text{Cj} = 7.656 \times 10^{-14} \ \text{F}

(2) 

\text{Nd} := 10^{16} \quad \text{tox} := 20 \cdot \text{nm} 

\phi_n := 60 \cdot \text{mV} \cdot \log \left( \frac{\text{Nd}}{\text{n}_i} \right) 
\phi_n = 0.36 

\phi_{pp} := -550 \cdot \text{mV} 

V_{FB} := \phi_n - \phi_{pp} \quad V_{FB} = 0.91 \ \text{V}

\begin{align*}
(\text{a}) & \quad \text{Xd}_{\text{max}} := \sqrt{\frac{2 \cdot \varepsilon_s \cdot (2 \phi_n)}{q \cdot \text{Nd}}} \quad \text{Xd}_{\text{max}} = 3.053 \times 10^{-5} \\
\text{Qb}_{\text{max}} & := q \cdot \text{Nd} \cdot \text{Xd}_{\text{max}} \\
\text{Cox} & := \frac{\varepsilon_{ox}}{\text{tox}} \\
V_{TP} & := V_{FB} - 2 \cdot \phi_n - \frac{\text{Qb}_{\text{max}}}{\text{Cox}} \quad V_{TP} = -0.093
\end{align*}
(b) 1V is greater than flatband voltage -> the MOS is in accumulation mode

(c) Maximum capacitance is simply Cox:
\[ C_{max} := Cox \quad C_{max} = 1.727 \times 10^{-7} \, \text{F/cm}^2 \]

(d) \[ C_{b_{min}} := \frac{\varepsilon_s}{X_{d_{max}}} \]
\[ C_{min} := \frac{Cox \cdot C_{b_{min}}}{Cox + C_{b_{min}}} \quad C_{min} = 2.835 \times 10^{-8} \, \text{F/cm}^2 \]

(3) -2V is more negative than threshold (-0.093V), so it is in inversion. The charge on the semiconductor side include a fixed donor charges from the semiconductor-oxide interface to the maximum depletion width, \( X_{d_{max}} \) and the inversion hole charges at the interface, \( Q_p \). The gate charge is equal to the total charge with opposite sign.

\[
\begin{align*}
V_{GB} &= -2 \\
Q_p &= -Cox \cdot (V_{GB} - V_{Tp}) \\
\rho_b &= q \cdot N_d \\
Qg &= -Q_p - \rho_b \cdot X_{d_{max}} \\
X_{d_{max}} &= 3.053 \times 10^{-5}
\end{align*}
\]

\[
\begin{align*}
V_{FB} &= 0 \\
V_{FB_{m}} &= \phi_n - \phi_m \\
\Delta V_{FB} &= V_{FB_{m}} - V_{FB} \\
V_{Tp_{m}} &= V_{Tp} + \Delta V_{FB}
\end{align*}
\]

(4) Flatband voltage and threshold voltage is shifted by the same amount:
\[
\begin{align*}
\phi_n &= 0 \\
V_{FB_{m}} &= \phi_n - \phi_m \\
V_{FB} &= 0.36 \\
\Delta V_{FB} &= V_{FB_{m}} - V_{FB} \\
\Delta V_{FB} &= -0.55 \\
V_{Tp_{m}} &= V_{Tp} + \Delta V_{FB} \\
V_{Tp_{m}} &= -0.643 \, \text{V}
\end{align*}
\]
\[
I_{DS} = \frac{W}{L} \times \mu_n \times Cox \times V_GS - V_Tn
\]

Since \(V_{DS} > V_{DS_{sat}}\), the FET is in saturation.

\[
V_{DS_{sat}} = V_{GS} - V_{Tn}
\]

(a) The NMOS FET is turned on when the gate voltage is equal to the threshold voltage

\[V_{Tn} = 0.353\]

(b) \(V_{GS} = 2\)

\[V_{DS} = 5\]

\[V_{DS_{sat}} = V_{GS} - V_{Tn}\]

\[V_{DS_{sat}} = 1.647\]

Since \(V_{DS}\) is greater than \(V_{DS_{sat}}\), the FET is in saturation.

\[
I_{DS}(V) = \frac{W}{L} \times \mu_n \times Cox \times (V_{GS} - V_{Tn})^2
\]

\[I_{DS}(5) = 6.789 \times 10^{-3} \text{ Amp}\]