University of California at Berkeley
College of Engineering
Dept. of Electrical Engineering and Computer Sciences

EE 105 Midterm I

Fall 2005       Prof. Borivoje Nikolić       October 13, 2005

Your Name: ____________________________
Student ID Number: _____________________

Guidelines
Closed book and notes; there are some useful formulas in the end of the exam.
You may use a calculator.
You can unstaple the pages with formulas, but do not unstaple the exam.
Show all your work and reasoning on the exam in order to receive full or partial credit.
Time: 80 minutes = 1 hour, 20 minutes.

Score

<table>
<thead>
<tr>
<th>Problem</th>
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<tr>
<td>1</td>
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<td>2</td>
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<td>3</td>
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<td>Total</td>
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1. Integrated charge-storage element [14 points]

The following figure shows the cross-section of a PMOS capacitor structure. P+ poly-silicon gate covers two regions: region A with gate oxide thickness of 300nm and region B with gate oxide thickness of 3nm respectively. The effective areas of the capacitor over the thick and thin oxide are 10.000μm² and 100μm² respectively. Please use the following parameters: \( \Phi_{p^+} = -550\text{mV}, \quad \varepsilon_{Si} = 11.7, \quad \varepsilon_{SiO_2} = 3.9, \quad \varepsilon_0 = 8.854 \times 10^{-14} \text{F cm}^{-1}, \quad n_i = 10^{10} \text{cm}^{-3}. \)

<table>
<thead>
<tr>
<th>400nm P+</th>
<th>300nm SiO₂</th>
<th>400nm P+</th>
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</thead>
<tbody>
<tr>
<td>Region A</td>
<td>( N_{\text{SUB}} = 10^{15} \text{cm}^2 )</td>
<td>Region B</td>
</tr>
<tr>
<td></td>
<td>( N_{\text{SUB}} = 10^{18} \text{cm}^2 )</td>
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(a) [4 points] What are the flat-band voltages \( (V_{FB}) \)'s of regions A and B?

\[
V_{FB\text{A}} = - (\Phi_{p^+} - \phi_n) = - (-550 - 25 \ln \left( \frac{10^{15}}{10^{10}} \right)) \text{mV} = 838 \text{mV}
\]

\[
V_{FB\text{B}} = - (-550 - 25 \ln \left( \frac{10^{10}}{10^{9}} \right)) \text{mV} = 1010 \text{mV}
\]

\[ W_{FB\text{A}} = 0.838 \text{V} \]

\[ W_{FB\text{B}} = 1.01 \text{ V} \]
(b) [4 points] What are the threshold voltages ($V_t's$) of regions A and B?

\[ V_{T1} = V_{T0} - 2\phi_n - \frac{1}{C_{ox}} \int A_{ox} E_i N_0 (2\phi_n) \]

\[ C_{ox} = \frac{E_{ox}}{E_{ox}} \]

\[ E_{ox} = E_{ox} E_0 \]

\[ E_i = E_i E_0 \]

\[ \phi_n = 0.925 \log \left( \frac{N_0}{n_0} \right) \]

\[ V_{TA} = -0.938 \text{ V} \]

\[ V_{TB} = -0.391 \text{ V} \]

(c) [5 points] Sketch the charge, E-field and potential distribution from $x = -400\text{nm}$ to $x = 400\text{nm}$ when $V_d = -0.5\text{V}$ for regions A and B. Assume that the potential at $x = -400\text{nm}$ is zero.
(d) [6 points] Sketch the CV of the whole capacitor structure. Please label the relevant points on the C- and V-axis.
2. Semiconductors, pn Junctions and MOS devices [20 pts]

A few useful constants: The permittivity of silicon is \( \varepsilon_s = 1.035 \times 10^{-12} \) F/cm and the permittivity of SiO\(_2\) is \( \varepsilon_{\text{SiO}_2} = 3.45 \times 10^{-12} \) F/cm. You can assume mobilities of \( \mu_n = 1500 \) cm\(^2\)/(Vs) and \( \mu_p = 500 \) cm\(^2\)/(Vs). The saturation electric field for electrons is \( E_{\text{sat}} = 1.25 \times 10^4 \) V/cm and their saturation velocity is \( v_{\text{sat}} = 10^7 \) cm/s. Unit charge: 
\( q = 1.6 \times 10^{-19} \) C, \( n_i = 10^{10} \) cm\(^{-3}\).

(a) [4 points] In a silicon resistor made from N-doped silicon doped to \( 10^{18} \) per cubic cm, with a length of 10\( \mu \)m, a width of 1\( \mu \)m, and a thickness of 0.1\( \mu \)m, what is the maximum current which can flow?

\[
I = A J = A \frac{n}{q} v_{\text{sat}}
\]
\[
= (0.1 \times 10^{-6}) \times 10^{-8} \times 1.25 \times 10^{-13} \times 10^7 \times 10^{-10}
\]
\[
= 0.0186 \text{mA} = 1.86 \text{mA}
\]

\[I_{\text{max}} = 1.6 \text{mA}\]

(b) [4 points] For a silicon PN junction at room temperature which has one side P doped to a concentration of \( 10^{18} \) per cm\(^3\) and the other side N doped to a concentration of \( 10^{16} \) per cm\(^3\), find the depletion depth into both the P side and into the N side.

\[X_{dP} = X_{dn} + \frac{N_D}{N_A} X_{dn} = X_{dn} \left(1 + \frac{N_D}{N_A}\right)\]

Use 
\[X_{dP} = \sqrt{\frac{2 q E_{\text{sat}}}{\phi}} \left(\frac{1}{N_A} + \frac{1}{N_D}\right) = 3.25 \text{nm}\]

(c) [4 points] What is the qualitative relationship between the width of the depletion region and the conductivity for the N side of the junction in part (b). Briefly explain.

\[X_{dn} \propto \frac{1}{N_A}, \quad \delta = \frac{X_{dn}}{X_{dP}} \propto \frac{N_D}{N_A} \propto N_A\]

With an increase in conductivity, depletion width increases [decreases] (circle one).
(d) [4 points] Consider two MOSFETs with identical dimensions, but with differently doped substrates; MOSFET A has the substrate doped with $N_A = 10^{19}$ cm$^{-3}$, and MOSFET B has doping of $N_A = 10^{16}$ cm$^{-3}$. Assume equivalent bias for both transistors, where both transistors are in saturation. In which case will the same change in $V_{DS}$ voltage ($\Delta V_{DS}$) cause a larger relative change in the capacitance between the drain and the substrate $\Delta C_d/C_d$. Explain your answer.

\[
C_j = \frac{C_{j0}}{1 - \frac{V_D}{\phi_{sa}}} \quad \Rightarrow \quad \frac{dC_j}{C_{j0}} = \left[ \frac{C_{j0}}{1 - \frac{V_D}{\phi_{sa}}} \right]^{-1} = C_j \left( -\frac{1}{2} \right) \left( 1 - \frac{V_D}{\phi_{sa}} \right)^{-\frac{3}{2}} dV_D
\]

\[
\Rightarrow \frac{\Delta C_j}{C_{j0}} = \frac{1}{2} \frac{V_D}{\phi_{sa}} \left( 1 - \frac{V_D}{\phi_{sa}} \right)^{-\frac{3}{2}} \Delta V_D
\]

\[
N_A \uparrow \Rightarrow \phi_{sa} \uparrow \Rightarrow A \downarrow, B \downarrow
\]

\[
\Rightarrow \Delta N_A \uparrow, \frac{\Delta C_j}{C_{j0}} \downarrow
\]

**MOSFET A** / **MOSFET B** (circle one)

(e) [4 points] Which one of the two MOSFETs from (d) would have a larger relative change in effective channel length, $\Delta L/L$, under the same change in $V_{DS}$ voltage ($\Delta V_{DS}$). Explain your answer.

\[
C = \frac{\varepsilon}{x}
\]

\[
\text{from } (d), \quad N_A \uparrow \Rightarrow \frac{\Delta C}{C} \downarrow \Rightarrow \frac{\Delta \varepsilon}{\varepsilon} \downarrow \Rightarrow \frac{\Delta L}{L} \downarrow
\]

**MOSFET A** / **MOSFET B** (circle one)
3. MOSFET circuit [16 points]

\[ V_{DD} \]
\[ i_{IN} \]
\[ M_1 \]
\[ M_2 \]
\[ V_{OUT} \]

Given:
- \( L_1 = L_2 = 0.5 \mu m \)
- \( W_1 = W_2 = 5 \mu m \)
- \( \mu C_{ox} = 100 \mu A/V^2 \)
- \( V_{Th} = 0.5 \text{ V} \)
- \( \lambda_n = 0 \text{ V}^{-1} \)
- \( \gamma = 0 \)

(a) [4 points] In which modes of operation are operating \( M_1 \) and \( M_2 \) for \( i_{IN} \neq 0 \)? Explain your answer.

- \( M_1 \) - saturation \( (V_{GD1} = 0 < V_{Th}) \)
- \( M_2 \) - linear \( (V_{GS2} = V_{Th1} > V_{Th}) \)
(b) [8 points.] Find the relationship \( v_{out} = v_{out}(v_{in}) \). You do not need to substitute the numerical values.

\[ v_{IN} = \left( \frac{W}{L} \right) \mu_{Cox} \left( V_{in1} - V_{TN} \right)^3 \]
\[ = \frac{K}{2} \left( v_{IN} - v_{out} - V_{TN} \right)^2 \quad (1) \]
\[ K = \frac{\mu_{Cox} W}{L} \]

\[ v_{IN} = \left( \frac{W}{L} \right) \mu_{Cox} \left( (V_{IN2} - V_{TN}) V_{OUT} - \frac{V_{IN2}}{2} \right) \]
\[ = K \left( (V_{in} - V_{TN}) V_{OUT} - \frac{V_{OUT}^2}{2} \right) \quad (2) \]

From (1),
\[ V_{IN} = \frac{2v_{IN}}{K} + V_{out} + V_{TN} \quad (3) \]

From (2),
\[ V_{IN} = \left[ \frac{2v_{IN}}{K} + \frac{V_{OUT}^2}{2} \right] V_{OUT} + V_{TN} \quad (4) \]

(3, 4) \Rightarrow
\[ \sqrt{\frac{2v_{IN}}{K} + V_{OUT}} = \frac{2v_{IN}}{K} V_{OUT} + \frac{V_{OUT}^2}{2} \]
\[ \therefore \quad V_{OUT}^2 + \frac{2v_{IN}}{K} V_{OUT} - \frac{2v_{IN}^2}{K} = 0 \]
\[ \therefore \quad V_{OUT} = \left( 2 - \sqrt{2} \right) \frac{v_{IN}}{2} \]
(c) [4 points] If the current source $i_D$ is implemented as simple DC-biased PMOS transistor ($W/L = 10$, $\mu_C = 100 \ \mu A/V^2$, $V_{dd} = -0.5 \ V$, $\lambda_p = 0 \ V^{-1}$, $\gamma = 0$), find the maximum and minimum values of $V_{out}$, under which the circuit operates correctly, with the supply voltage of $V_{dd} = 5\ V$.

From b)

- $i_D \to 0$, $V_{out} \to 0$ ($M_1, M_2$ barely $ON$)

$V_{out, \min} = 0 \ V$

When $V_B \to i_D \uparrow \to V_{out} \uparrow$,

$MP$ is still in saturation as long as

$V_B > -V_{th} + V_{ol}$

When $V_{out}$ is max, $V_B = V_{in} - V_{th} - V_{ol}$

$V_{out, \max} = \frac{K}{2} (V_{oo} - V_{th} - V_{ol})^2 = \frac{K}{2} (V_{oo} - V_{in})^2$

$V_{out} = (2 - \sqrt{2}) \sqrt{\frac{i_D}{2C}}$

$= (\sqrt{2} - 1) (V_{oo} - V_{in}) = (\sqrt{2} - 1) V_{ov}$

On the other hand, $V_{out} = V_{oo} - 2V_{in} + V_{tn}$

$V_{ov} = \frac{V_{out} - V_{in}}{2}$

$V_{out, \min} = 0 \ V$

$V_{out, \max} = 0.772 \ V$