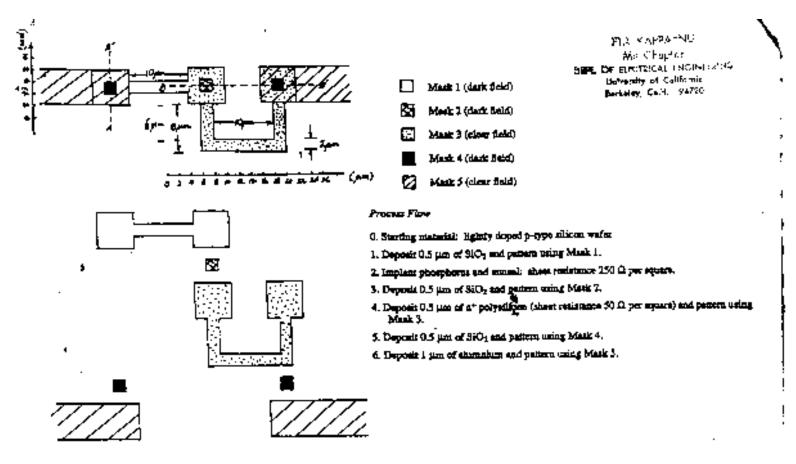
EE 105, Fall 1996 Midterm #1 Professor R.T. Howe

Problem #1

The CAD layout for a resistor is shown below, followed by the individual layou patterns.



(a) [5 pts.] Given that the "dogbone" contact regions used for both the implanted resistor and the polysilicon resistor contribute 0.6 squares and that the corners contribute 0.56 squares, find the resistance between the metal lines in kilo-ohms.

(b) [6 pts.] Accurately sketch the fabricated structure along the cross section A - A' for this CAD layout and process flow. Use the horizontal line below as the silicon surface; the dimensional scale along it corresponds to the appropriate scale on the CAD layout. The vertical scale should be followed in sketching the deposited layers. Also, label all layers and use the "dot" fill pattern from Mask 3 for polysilicon layers and the "slash" fill pattern from Mask 5 for metal layers.

(c) [7 pts.] Accurately sketch the fabricated structure along the cross section B - B' for this CAD layout and

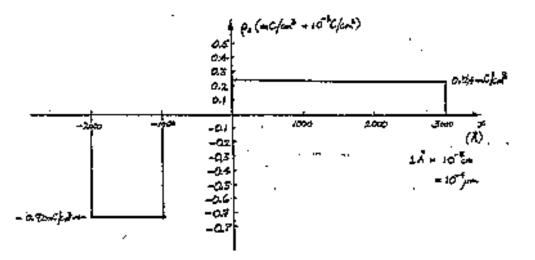
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process flow. Use the horizontal line below as the silicon surface; the dimensional scale along it corresponds to the appropriate scale on the CAD layout. The vertical scale should be followed in sketching the deposited layers. Also, label all layers and use the "dot" fill pattern from Mask 3 for polysilicon layers and the "slash" fill pattern from Mask 5 for metal layers.

Problem #2

Silicon-Oxide-Silicon Equilibrium Electrostatics [17 points] Given: $Eox = 3.9 \ Eo = 3.45 \ x \ 10^{-13} \ F/cm,$ $q = 1.6 \ x \ 10^{-19} \ C,$ $Es = 11.7 \ Eo = 1.04 \ x \ 10^{-12} \ F/cm,$ $1 \ A = 10^{-8} \ cm$

We have a sandwich of silicon (extending over x < -1000 A), silicon dioxide (extending over -1000 A $\leq x < = 0$ A), and silicon (extending over x > 0 A). The charge density Po(x) in the silicon-oxide-silicon sandwich in thermal equilibrium is given in the plot below.



(a) [3 pts.] From the charge density plot, identify type (n or p) of the right-hand silicon region (extending over x > 0 A) Justify your answer.

(b) [4 pts.] Find the numerical value of the electric field Eo (x = 0+), just inside the right-hand silicon region.

(c) [6 pts.] Plot the electric field Eo(x) in thermal equilibrium through the structure on the graph below.

(d) [4 pts.] What is the capacitance C(0) of this structure in thermal equilibrium (zero volts DC applied)? *Hint*: although you haven't seen this structure before, the reasoning behind the MOS and pn junction capacitors applies.

Problem #3

Short-Channel MOSFET model [15 points]

Given: new (and artificial!) model for an n-channel MOSFET with submicron channel lengths: Cutoff: iD = 0A, where Vgs < VtnTriode: $iD = WCoxVsat(Vds)(1 + BETA Vds^2)$, where Vgs >= Vtn, Vds < Vgs-Vtn Saturation: $iD = WCoxVsat(Vgs - Vtn)(1 + BETA Vds^2)$, where Vgs >= Vtn, vDS >= Vgs - Vtnwhere Vtn = 1.5 V, $BETA = 0.004 V^{-2}$, $Vsat = 10^{7} cm/s$, $Cox = 5 x 10^{-7} F/cm^2$, W = 10 um.

(a) [2 pts.] The MOSFET is biased at the operating point Vgs = 2.5V, Vds = 2V. What is the numerical value of the drain current iD?

(b) [3 pts.] Plot the drain current iD versus vDS, for Vgs = 0, 1, 2, 3, 4, and 5V on the axes below. You can set BETA = 0 for this part.

(c) [5 pts.] For the operating point in part (a), where Vgs = 2.5 V, Vds = 2V, what is the numerical value of the small-signal transconductance gm of this short-channel MOSFET?

(d) [5 pts.] For the operating point in part (a), where Vgs = 2.5 V, Vds = 2V, what is the numerical value of the small-signal output resistance ro of this short-channel MOSFET?

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