Ground Rules:

- Close book; one $8.5 \times 11$ crib sheet (both sides)
- Do all work on exam pages
- Default bipolar transistor parameters:
- $n p n: \beta_{\mathrm{n}}=100, \mathrm{~V}_{\mathrm{An}}=50 \mathrm{~V}, \mathrm{~V}_{\mathrm{CE}-\mathrm{sat}}=0.2 \mathrm{~V}$
- p np: $\beta_{\mathrm{p}}=50, \mathrm{~V}_{\mathrm{Ap}}=25 \mathrm{~V}, \mathrm{~V}_{\mathrm{EC}-\mathrm{sat}}=0.2 \mathrm{~V}$
- Default MOS transistor parameters: note LAMBDA depends on L!
- NOS: $\mathrm{MU}_{\mathrm{n}} \mathrm{C}_{\mathrm{ox}}=100 \mathrm{e}-6 \mathrm{~A} / \mathrm{V}^{2}$, LAMBDA $_{\mathrm{n}}=[0.1 / \mathrm{L}] \mathrm{V}^{-1}$ (L in micrometers) $\mathrm{V}_{\mathrm{Tp}}=1 \mathrm{~V}$
- PMOS: $\mathrm{MU}_{\mathrm{p}} \mathrm{C}_{\mathrm{ox}}=50 \mathrm{e}-6 \mathrm{~A} / \mathrm{V}^{2}$, LAMBDA $_{\mathrm{p}}=[0.1 / \mathrm{L}] \mathrm{V}^{-1}$ (L in micrometers) $\mathrm{V}_{\mathrm{Tp}}=-1 \mathrm{~V}$


## Problem \#1: Small-Signal Amplifier [24 points]


a) [4 pts.] What is width of transistor $\mathrm{M}_{2}$ such that the DC output voltage $\mathrm{V}_{\text {out }}=0 \mathrm{~V}$ for $\mathrm{V}_{\text {IN }}=0 \mathrm{~V}$. Given: the length of $\mathrm{M}_{2}$ is $\mathrm{L}_{2}=2 \mathrm{e}-6 \mathrm{~m}$.
$\mathrm{W}=\mathbf{1 0 0}$ micrometers
b) [ 4 pts.] What is the numerical value of the input resistance $R_{\text {in }}$ of this amplifier? Your answer should be correct to within +/- $5 \%$.
If you couldn't solve (a) you can assume for this part that $\mathrm{W}_{2}=25 \mathrm{e}-6 \mathrm{~m}$. Of course, this isn't the correct answer to part (a).

## $\mathbf{R}_{\text {in }}=\mathbf{1 4 . 3 1}$ mega-ohms

c) [4 pts.] What is the numerical value of the output resistance $\mathrm{R}_{\text {out }}$ of this amplifier? Your answer should be correct to within +/- $5 \%$.
If you couldn't solve (a) you can assume for this part that $\mathrm{W}_{2}=25 \mathrm{e}-6 \mathrm{~m}$. Of course, this isn't the correct answer to part (a).

## $\mathbf{R}_{\text {out }} \mathbf{= 2 6 0}$ ohms

d) [6 pts.] What is the numerical value of the overall voltage gain $\mathrm{v}_{\text {out }} / \mathrm{v}_{\mathrm{s}}$, with $\mathrm{R}_{\mathrm{s}}=100$ kilo-ohms and $\mathrm{R}_{\mathrm{L}}=20$ kilo-ohms? Your answer should be correct to within $+/-5 \%$.
Again, If you couldn't solve (a) you can assume for this part that $\mathrm{W}_{2}=25 \mathrm{e}-6 \mathrm{~m}$. Of course, this isn't the correct answer to part (a).
$\mathrm{A}_{\text {v-overall }}=\mathbf{0 . 9 8 0 4}$
e) [6 pts.] Sketch the transfer curve $\mathrm{V}_{\text {OUT }}$ versus $\mathrm{V}_{\text {IN }}$ for $-2.5<=\mathrm{V}_{\text {IN }}<=+2.5 \mathrm{~V}$ on the graph below. For this part, $R_{L}$ is infinity and $R_{S}=0 \mathrm{~V}$.
Hint: you should note that the current supplies each require at least $\mathrm{V}_{\mathrm{SUP}(\min )}=0.5 \mathrm{~V}$ in order to function.


## Problem \#2: Digital Logic Gate [14 points]


a) [2 pts.] What is the logic operation performed by the above circuit? In other words, what is the logical expression for Q in terms of the three inputs $\mathrm{A}, \mathrm{B}$ and C ? Q=(A-bar + B-bar) dot C-bar
b) [ 4 pts.] The graphs below plot the voltage waveforms over an interval of 35 microseconds. Fill in the output voltage waveform $\mathrm{v}_{\mathrm{Q}}(\mathrm{t})$ over $0-=>35 \mathrm{e}-6 \mathrm{~s}$. Note that the rise and fall times are essentiall zero on this time scale.

c) [4 pts.] Find the numerical value of the best case low-to-high propagation delay ( $\mathrm{t}_{\mathrm{PLH}}$ ) for this logic gate.
$\mathbf{t}_{\mathbf{P L H}}=\mathbf{0 . 7 5} \mathbf{n s}$
d) [4 pts.] Find the width of the $n$-channel transistor such that the high-to-low propagation delay $\left(\mathrm{t}_{\mathrm{PLH}}\right)$ is equal to your answer for part c). If you couldn't answer part c) you can assume for this part that $\mathrm{t}_{\mathrm{PLH}}$ (best) $=1 \mathrm{~ns}=10^{-9} \mathrm{~s}$.
$\mathrm{W}=6.665$ micrometers

## Problem \#3: Bipolar Transistor Physics [12 points]

NOTE: The default npn transistors do not apply for this problem!


GIVEN:
$\mathrm{N}_{\mathrm{dE}}=2 \times 10^{18} \mathrm{~cm}^{-3}$
$\mathrm{N}_{\mathrm{dB}}=10^{17} \mathrm{~cm}^{-3}$
$\mathrm{N}_{\mathrm{dC}}=10^{16} \mathrm{~cm}^{-3}$

The base and emitter widths are $\mathrm{W}_{\mathrm{B}}=\mathrm{W}_{\mathrm{E}}=0.5$ micrometers. The electron diffusion coefficient in the base is $\mathrm{D}_{\mathrm{nB}}=10 \mathrm{~cm}^{2} / \mathrm{s}$ and the hole diffusion coefficient in the emitter is $\mathrm{D}_{\mathrm{pE}}=5 \mathrm{~cm}^{2} / \mathrm{s}$.
a) [3 pts.] Qualitatively sketch the minority carrier concentrations in the emitter, base and collector on the graph below, assuming that the transistor is biased in the forward active region.

b) [3 pts.] For $\mathrm{V}_{\mathrm{OUT}}=0 \mathrm{~V}$ what is the numerical value of the minority electron concentration at $\mathrm{x}=0, \mathrm{n}_{\mathrm{pB}}$ (0)? You can assume that the transistor is biased in the forward active region.

## Not available

c) [3 pts.] What is the numerical value of the base current $\mathrm{I}_{\mathrm{B}}$ for the bias condition in part b)? If you couldn't solve b) assume for this part that $n_{p B}(0)=10^{15} \mathrm{~cm}^{-3}--$ not the correct answer to $b$ ), of course.

## $\mathrm{I}_{\mathrm{B}}=\mathbf{2 . 5} \mathbf{~ m i c r o - a m p s}$

d) [3 pts.] What is the numerical value of $\mathrm{V}_{\text {IN }}$ in order that the transistor is biased in the forward active region with $\mathrm{V}_{\text {OUT }}=0 \mathrm{~V}$ ?
Notes: You cannot assume that $\mathrm{V}_{\mathrm{BE}}=0.7 \mathrm{~V}$ for this part. If you couldn't solve parts b) and c) you can assume that $\mathrm{n}_{\mathrm{pB}}(0)=10^{15} \mathrm{~cm}^{-3}$ and that $\mathrm{I}_{\mathrm{B}}=4$ micro-amps. Neither of these answers are correct, of course. $\mathbf{V}_{\mathbf{I N}}=\mathbf{3 . 2 7 7} \mathbf{~ V}$

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